AMD-K6® Processor

EMI DESIGN CONSIDERATIONS

Application Note

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Revision History

Date	Rev	Description
Mar 1999	A	Initial published release.
Feb 2000	B	Misc. additional ideas added.
Apr 2000	C	Corrected Example 1 in “Calculating Required Number of Capacitors” on page 31.

Application Note

AMD-K6®

Processor EMI Design Considerations

Introduction

The AMD-K6® processor family consists of high-performance x86-compatible processors containing more than 8.8 million transistors. The previous generation of AMD-K6 processors used 2.9 V and 3.2 V to power the processor's core circuitry. They were fabricated using AMD's enhanced 0.35-µm process technology (CS34EX). The newer generation of processors uses 2.2 V, and is manufactured by the CS44E 0.25-µm process. The I/O portion of all the processors operates at the industry-standard 3.3 V.

This application note is intended to guide the board and system designer through developing a layout that meets FCC and CISPR class B regulations. A total systems solution approach is key to achieving an EMI compliant system. Care must be given to the choice of components, PC board (layout), chassis (including power supply), and cables.

This application note focuses on PC board design issues. Other issues will be discussed in more detail in another application note.

The designer should use good high-frequency design practices in order to minimize EMI. It is important to address EMI issues

early in the design stage. It is usually more difficult to fix EMI problems late in the design process.

This application note makes many suggestions to reduce EMI. Some may not be usable in the reader's situation, due to space or cost constraints. The designer must decide which techniques to apply.

Electromagnetic Interference (EMI)

Every switching circuit emits electromagnetic radiation other than its intended output. This unintended output becomes electromagnetic interference (EMI) for other nearby circuits. EMI strength is related to the amplitude of the current and voltage. The larger the current or higher the voltage — the stronger, potentially, is the interference.

Three Basic Elements of EMI

The first element of EMI is current from an emitting source, called a culprit. Culprits can be an unterminated line, an impedance discontinuity, an oscillator, a clock, or a switching power supply.

The second element is the transfer method, or coupling media. A coupling can be antenna-to-antenna (radiation), field-to-wire or wire-to-field (crosstalk), or common ground impedance (conduction).

The third element is a receiving element, or victim. A victim can be a radio receiver, a television set, analog sensors, amplifiers, memories, disk drives, and so on.

EMI is an electric or electromagnetic field emitted from a culprit, transferred by coupling media to a victim, where it degrades that signal.

Radiation Transfer

Currents that generate radiated fields are of two kinds—common mode and differential mode.

Common Mode. Common-mode currents are high-frequency current transients generating significant Radio Frequency (RF) potentials due to inductance in the plane or wire. They are present in both the V_{CC} and ground planes, in both wires of a differential pair, or in both the shield and center wire of a coaxial cable. These currents are very difficult to measure because the ground plane may contain the common-mode signals, so they cannot be measured relative to ground. A common-mode choke is usually the most effective way to filter these unwanted currents.

Differential Mode. Differential mode currents are high-frequency current transients in a trace, wire, or plane. They can be measured relative to ground, for instance, between the V_{CC} plane and ground or between a signal and ground. Differential-mode current can be effectively shielded.

Antennas

The second ingredient necessary for radiation is an antenna. Antennas can be cables, slots in a chassis, traces on a PC board, and so on. To understand antenna radiation, imagine running an alternating current through a simple loop of wire (see Figure 2). The magnitude of radiation from the loop varies proportionally to the current. The radiated field intensity is maximal in the plane of the loop.

CrossTalk is induced when a transition on an adjoining signal causes an unintentional signal on the victim net.

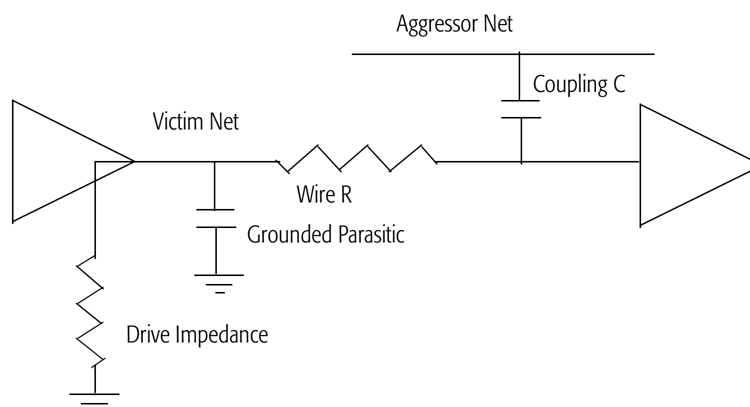


Figure 1. Crosstalk Model

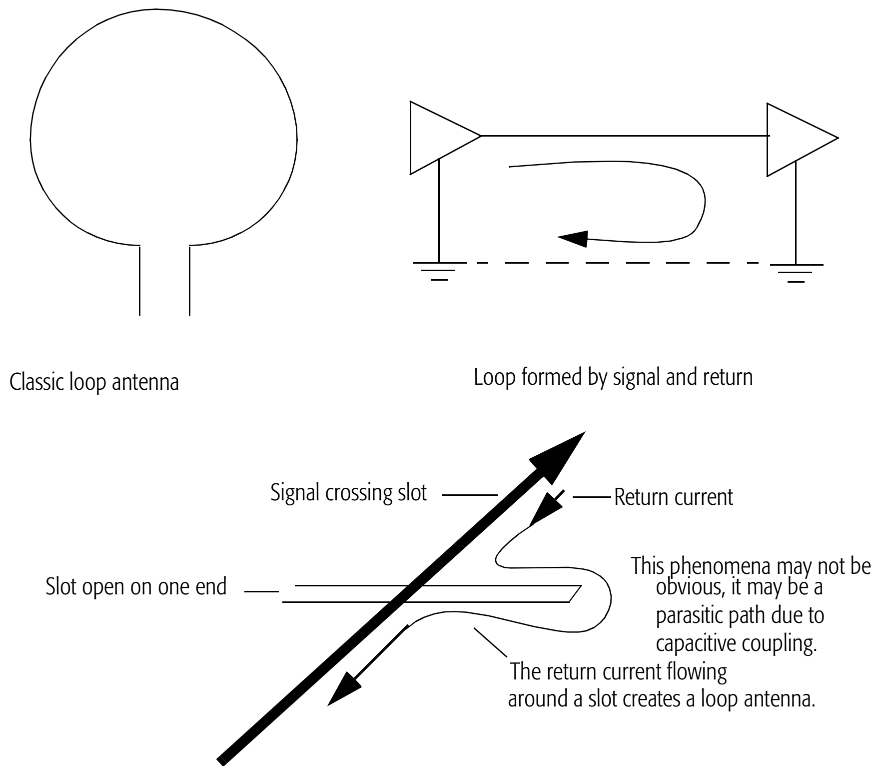


Figure 2. Loop Antennas

One of the principal techniques for reducing EMI is to build PC boards with signals running over a ground plane. This reduces loop area. The closer the trace is to the ground plane, the smaller the loop. When a trace crosses a break in a plane the loop area is increased (see Figure 3 on page 5).

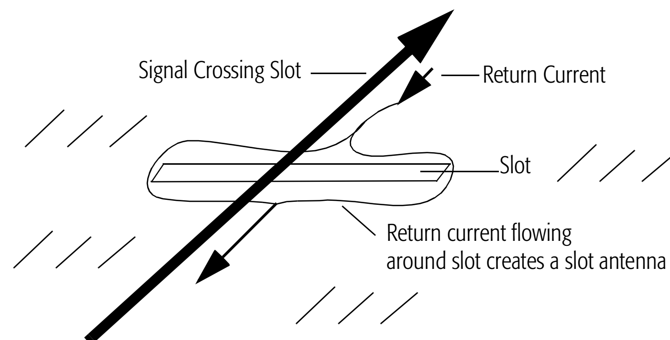


Figure 3. Antenna Formed by a Trace Crossing a Slot

A trace that extends past a reference plane creates a dipole antenna (see Figure 4).

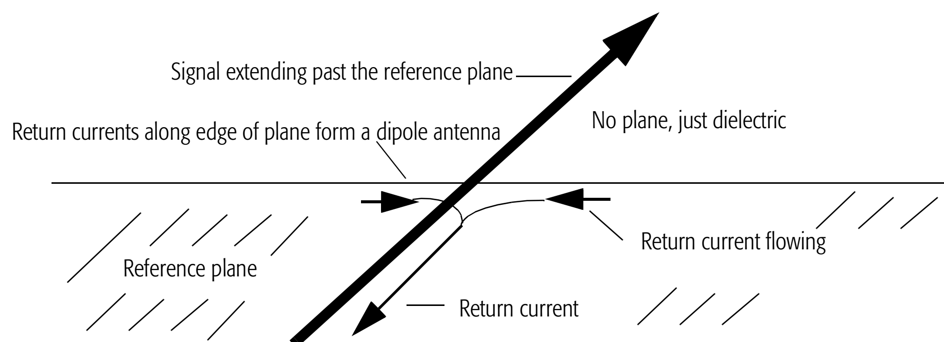


Figure 4. Dipole Antenna

A rectangular metal tube, such as a drive bay, creates a waveguide antenna (see Figure 5).

This box represents a drive bay which can act as a wave guide. The arrows represent EM fields.

Figure 5. Waveguide Antenna

Emission Strength

Emissions are proportional to current, area, and frequency.

If E = electric field (emission), I = current; A = area of loop; r = distance; L = antenna length; and F= frequency, then:

For differential mode: $E \sim IAF^2/r$

For common mode: $E \sim ILF/r$

Emissions are proportional to F^2 for differential mode and proportional to F for common mode. It might seem, therefore, that common mode radiation is easier to deal with than differential mode radiation because the emission increases with F rather than F^2. In fact, common mode is the more common culprit because in common mode the return current path is usually the earth ground or chassis skin, so the loop area is large and the radiation more serious. In differential mode the return current is in the adjacent wire and the loop area is small.

High Frequencies

High frequencies radiate more efficiently. Their wavelength is shorter than low frequencies so their waves can pass through smaller holes and can use smaller antennas for a given amount of radiation. Antenna loop area is the single most important attribute that a designer can control. However, because higher frequencies are very directional, they can be easier to shield than lower frequencies.

Locating the Source of EMI Using Harmonics

To determine the source of a radiated peak, divide its measured frequency by 2, 3, 4, and so on, until the frequency matches one of the system frequencies. In a personal computer those frequencies are usually:

- Real time clock — 32 kHz
- ISA bus — 7–8 MHz
- OSC clock — 14.31818 MHz
- PCI clock — 33.33 MHz
- Memory bus — 50 MHz, 60 MHz, 66.66 MHz, 75 MHz, 83.3 MHz, 95 MHz, or 100 MHz
- CPU core clock — 300 MHz, 350 MHz, 333 MHz, 380 MHz, 366 MHz, and 400 MHz
- Local bus clocks — 50 MHz, 60 MHz, 66.66 MHz, 75 MHz, 83.3 MHz, 95 MHz, or 100 MHz

Table 1. Bus Frequency / Multiplier / Resultant Core Frequency

	Bus Multiplier (Core Frequency)							
Bus Speed	**2.5**	**3.0**	**3.5**	**4.0**	**4.5**	**5.0**	**5.5**	**6.0**
50								
60								
66.6		200	233	266	300	333	366	400
75								
83.3								
95			333	380				
100		300	350	400				

Notes:
The filled-in values in this table represent frequencies associated with past and current AMD products.

Controlling EMI

The concepts introduced in this section are explained in more detail in subsequent sections of this application note.

Identifying the cause of EMI is usually easy. Fixing the situation is often difficult. Once the EMI source is identified, several remedies are possible. The source can be shielded or filtered. Coupling can be reduced. If loop area is the problem, rethinking the board layout can minimize it. The culprit's rise/fall time might be reduced, eliminating some of the higher harmonics. (Remember a square wave consists of the sum of a fundamental frequency and its odd harmonics. Reducing the edge rate reduces the higher frequency harmonic components.)

At the Emitting Source

The most common EMI source is a clock signal. Clocks are the strongest source of high-frequency current movement in digital circuits. To control emissions due to clocks:

- Place any pullup resistors used near the driver (source). Pullup resistors at the receiver (destination) increase the loop area.
- Keep clock traces short to minimize lead inductance and loop area.
- Keep clocks away from I/O lines to prevent coupling.
- Soften clock edges with series termination or resistor-capacitor (RC) filtering as needed.

Use a multilayer printed circuit board (PCB) without cutting the ground plane. Breaks in the ground plane increase printed circuit trace impedance and are also an impedance discontinuity.

Employ careful power-supply decoupling. For instance:

- Decouple each component's V_{CC} lead
- Use low equivalent series resistance (ESR) capacitors
- Bulk decouple application-specific integrated circuits (ASICs), processors, and the DC–DC converter input
- Filter I/O signals with damping resistors and ferrite beads
- Filter high-frequency components

Shielding the Chassis

Correct PC chassis design is an effective way to control emissions. The PC chassis is a shield for the PC board and the other noise sources in a computer. The shield performance of the chassis is determined by its conductivity and permeability. Conductivity (see “Shielding” on page 18) of the chassis affects its ability to reflect electric fields. Permeability affects its ability to absorb magnetic fields.

Seams and holes in the chassis often leak (radiate) energy and are potentially major EMI culprits. For instance, empty drive bays become slot antennas. Metal or conductive coated plastic filler panels are good solutions for blocking radiation from the drive bays. Be sure the various chassis pieces make electrical contact. A welded chassis is preferred to a riveted chassis because of the better electrical contact between parts.

Avoid a PC chassis with the following characteristics, all of which encourage EMI:

- Oxidized or painted steel pieces
- Non-conductive anodizing aluminum forms
- Long cracks and seams
- Large ventilation holes—both round and slotted
- Few PC board grounding points

A good chassis is key to controlling EMI. A good chassis should be made of steel with spring-metal gaskets or interlocking seams, have a filtered AC power entry, and have metal covers for unused bays or slots. As a general rule, the impedance should be less than 30 milliohms between chassis components. This resistance can be measured with a milliohm meter commonly used to isolate shorted traces on a PC board.

Correct Cabling

Cabling is another key component that can affect system EMI. Cables may have to contain ferrite beads or be shielded. Connectors may need to be shielded or to have internal filters. When possible, use twisted pair wires so that the field will cancel. Some of the worst EMI offenders are wires that exit the metal frame of the chassis but are inside the exterior cover, such as LEDs, reset switch wires, and the power switch wire.

Filtering I/O Signals

In the event that I/O signals become an unacceptable source of EMI, board layout should be designed to accommodate I/O signal filtering so that the appropriate type of filter can be easily added with a minimal amount of board rework. If the filters are not needed, the inputs and outputs of the filter can simply be shorted. Depending on the function and available board space, different types of filtering can be employed. Often times a capacitor to Frame ground, a simple series resistor, or a capacitor to DC common can solve the problem. Series ferrite beads are effective on signals to the keyboard and serial ports. An RC filter, Pi filter or T filter are often the preferred solution for the parallel port (see Figure 6). Common-mode chokes, most commonly used with networking devices such as Ethernet, can be used on I/O port signals and grounds.

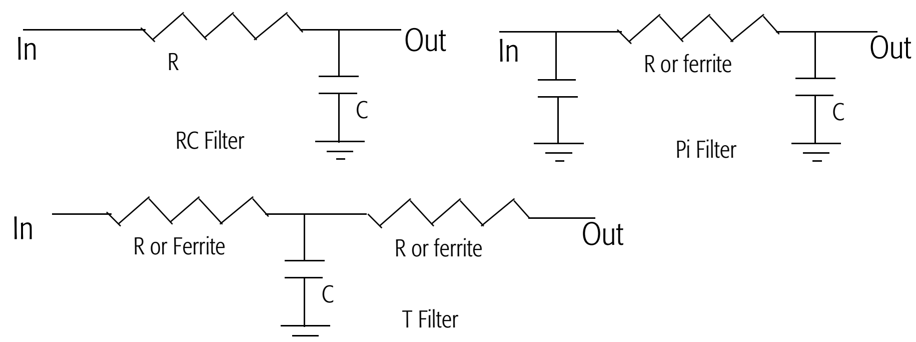


Figure 6. Filtering Techniques

Components that Influence EMI

General Component Selection Criteria

Many of the faster technologies used today to implement logical functions induce high current transients which can generate more di/dt noise emitted from a signal. In addition, these larger current transients can degrade signal quality by contributing to signal ringing which can also adversely affect EMI radiation. While selecting slower-speed technologies can alleviate radiation due to these particular sources, it is often not practical because of the requirements of the application, or because the desired function(s) are integrated into higher-level components, thus restricting the designer's choice. The designer is encouraged to request EMI data from the component vendor to assist in making the proper technology choice.

The following components can generate EMI:

- Processor
- Chipset
- Clock chip
- Power supplies: AC-DC and DC-DC
- Chassis
- Memory
- Cables and connectors
- Peripherals

Processor

The processor can be the source of some EMI problems. It is usually the highest frequency device in a system. It also has a large number of outputs switching.

At these high frequencies, it is important to minimize structures that will produce gain by resonating. Some of these structures are extremely difficult to identify. Others are straightforward. For example, slots and holes in the chassis can act as effective antennas, so look for ways to seal gaps. Empty drive bays are often overlooked culprits. Clock lines going to unpopulated SDRAM sockets should be turned off. Any signal exiting the box via a cable should be filtered. Often the more obscure coupling paths must be debugged by trial and error while measuring the system for radiation.

Processor, Package, and Heatsink

AMD has done EMI testing on its processors and has minimized their EMI contribution by a combination of on-chip and in-package decoupling capacitors and care in package design. These measures help, but it is still necessary to exercise thought and caution in board and system design. Noise can radiate from the processor lid or heatsink and couple into other components. Even the orientation of the heatsink can influence the amount of radiation.

The processor package lid can also act as an antenna (it is not grounded). Heatsinks can make an effective antenna. Provide a means to ground the heatsink if needed. Grounding to the chassis (lowest impedance) is usually preferred. However, grounding to the PC board is also effective. Other possible solutions are the SIL-PAD EMI shield from Bergquist or the Flex-Suppressor from Tokin. Either shield is placed between the processor and the heatsink, and absorbs the magnetic field component. (AMD has not used these particular solutions.)

Frequency Harmonics

The second and fourth harmonics usually contain the most energy. Therefore, for a system with a 300-MHz processor, 600 MHz and 1200 MHz are often the main problem areas. Harmonics of the bus frequency are also of concern. Bus speeds can be 66.6 MHz, 75 MHz, 83 MHz, 95 MHz, or 100 MHz. Sometimes it is difficult to determine the source of a noise peak as there are several oscillators in a PC. It may be necessary to divide the problem peak frequency by each of the known frequency sources to determine what harmonic of which source is the cause. For example, 475/95 = 5, so a 475 MHz signal is likely the fifth harmonic of a 95 MHz bus signal.

Core Voltage Filtering

Adding an EMI filter (see Figure 7 on page 13) at the input to the DC–DC converter generating the core voltage usually helps to decrease EMI. Good high-frequency (0.01 µF and 0.001 µF) ceramic capacitors across V_{CC2} (V_{core}) are important. Be aware of the magnetic saturation current of the inductor chosen. Ensure the DC resistance of the coil is as low as possible. Choosing the wrong inductor can cause a worse problem than not having one.

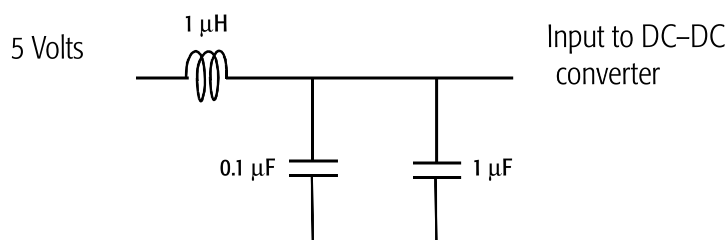


Figure 7. Processor Core Power Supply EMI Filter

Remember that radiation efficiency is dependent on the wavelength of the frequency, and higher frequencies radiate better. Filtering these frequencies at the source is the most effective technique for controlling EMI.

VRM Cards

Coupling between heatsinks and VRM (Voltage Regulator Module) cards can occur. This coupling can be minimized by orienting the ground plane side of the card towards the processor. If this is impractical the designer may want to add a shield between the VRM card and the processor.

Ensure the switching regulator's inductor is rated for a higher instantaneous current than needed. (Allow for up to twice the rated current of the power supply.) If the current exceeds its magnetic saturation point, processor harmonic noise will be passed through the inductor to the 5-V plane.

Chipset and Clock Chip EMI

High-frequency clocks can be a major contributor to EMI, so consideration should be given to terminating all clocks on the board. A ferrite bead (surface mounted) or a series resistor installed as close as possible to the source can be included in all clock signals to minimize radiation. Parallel termination—such as a capacitor and resistor in series to ground or a Thevenin pull-up/pull-down resistor—is a better solution if the clock trace is long relative to its rise/fall time (where long is defined as ">(2.5 in/ns) * T (ns)"). For example, any clock trace longer than 2.5 inches with a rise time of 1.0 ns should be parallel terminated.

To assist with the proper selection of the termination technique, as well as the component value selection, it is

recommend that every clock circuit be modeled with an appropriate simulator such as signal integrity tools from Mentor, Cadence, and Viewlogic, or with the classic analog simulator SPICE. IBIS models can be obtained from most component vendors to do these simulations. Most tools focus on signal integrity. However, good signal integrity is a necessary condition for reduced EMI. Current EMI specific tools are not very accurate but can give the designer an idea where problems may exist.

One of the best approaches is to get recommendations from the chip manufacturers, and check if they have any measured data.

Clock chips have clocks going to each SDRAM module. Many clock chips use the I^2C bus for control. If there are sockets with SDRAM not installed, the clocks to these sockets should be disabled via the I^2C interface.

Spread-Spectrum Clock Generation

Spread-spectrum clock generation (SSCG) is a very useful technique to reduce EMI. It distributes energy over several frequencies rather than concentrating it at one frequency, thereby reducing the EM profile by varying the clock frequency slightly. It is a key technique for high-speed systems, and is especially useful in portable systems because it reduces the shielding required.

Figure 8 on page 15 shows the effects of SSCG, that is, the theoretical reduction in emissions as a function of frequency and the modulation percentage of the frequency. The reduction in emissions is given by the equation:

$$\text{dB reduction} = 6.5 + 9\log_{10}P + 9\log_{10}(\text{Freq in MHz}),$$

where P is defined as the percent reduction in emissions, such that:

```
P = (percent modulation)*(bus frequency multiplier) *
(harmonic number)
```

For example:

```
P = 0.5% Mod * 3 x BF * 4th Harmonic
results in a 6% reduction of emissions.

P = 3% Mod * 3 x BF * 4th Harmonic
results in a 36% reduction of emissions.
```

The benefits of SSCG are more pronounced at higher frequencies.

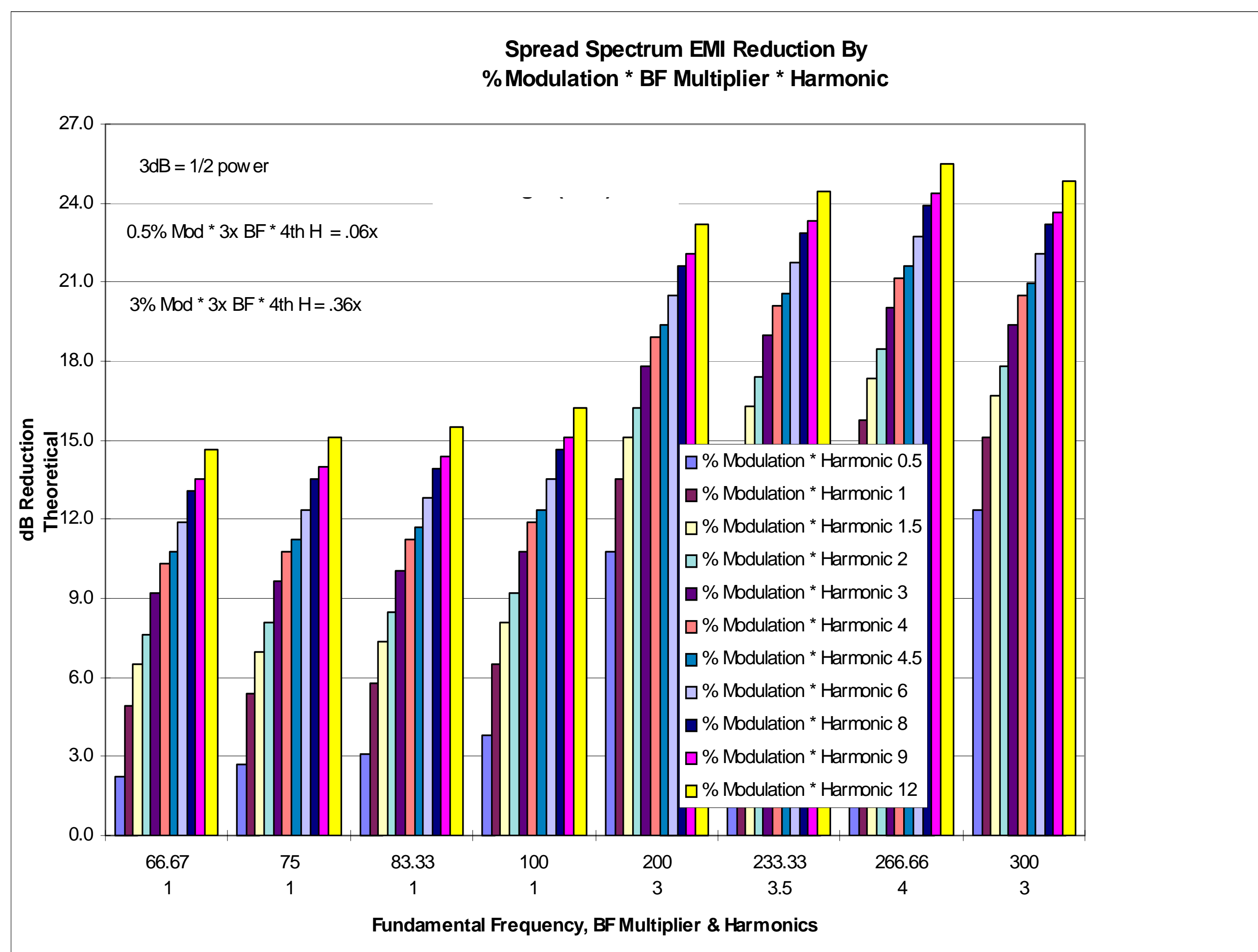


Figure 8. Effects of Spread Spectrum Clocking

When using SSCG, it is important to verify that other components (Northbridge, SDRAM, etc.) containing PLLs are able to track the frequency change. The AMD-K6 processor PLL is compatible with SSCG, but some motherboards and chipsets may not be.

Many manufacturers of clock chips offer SSCG capability. The following vendors supply spread-spectrum clock chips:

- International Microcircuits Inc. (IMI)
- IC Works
- Integrated Circuit Systems (ICS)

Memory

As memory speed increases and buses get wider, the amount of noise generated by memory becomes a significant contribution to total EMI.

The most important consideration for a board designer to minimize EMI due to memory is to have good decoupling near the memory sockets. It is also important to keep the traces from the memory controller to the Dual Inline Memory Module (DIMM) sockets as short as possible.

Sometimes changing from one brand of memory to another can have a pronounced effect. This is partially due to decoupling and layout on the module but can also depend on the brand of DRAM used.

AC Power Supply

Often designers focus on radiated noise, but conductive noise is also an important part of meeting regulatory requirements. Conducted emissions (below 30 MHz) occur through the AC power line. The AC line cord can pick up radiated emissions and pass them down the line. It can also conduct internally generated noise from inside the chassis down the power cable. The best practice is positioning a line filter near the exit point of the line cord.

Some power supplies have an EMI filter built in, but many do not. Choose a power supply that has a built-in EMI filter. This is often overlooked. A good power entry filter is usually the easiest way to meet conductive EMI requirements. In general, power supplies with poor bulk and/or high-frequency decoupling usually fail EMI testing.

Chassis Design

Chassis parts should be in good electrical contact with each other. It is important to keep impedance less than 30 milliohms between chassis parts. Impedance greater than 75 milliohms will lead to EMI problems.

- Covers and fascias leak when not grounded. A chassis design that has wide overlapping cover contacts can have poor impedance contact.
- Be aware of the possibility of long, narrow gaps in the chassis, perhaps caused by a bend in the chassis cover or a long seam. These gaps, although sometimes difficult to see, can become large antennas.
- The effective length of a long gap or seam can be reduced by adding intermediate ground points. Welded seams (impedance less than 30 milliohms) are preferred to riveted seams (impedance greater than 70 milliohms). It is also possible to use grounding metal gaskets on seams.
- Avoid having oxidation or paint at grounding (contact) points. Be aware of paint that may be preventing different chassis pieces from making an electrical connection.
- High contact impedance of ISA/PCI slot covers is very common. Slot covers should not be painted. It is preferred that they be held in place by a screw, not just a clip. The top of the cover should have an angular detent to bite into the chassis when the screw is tightened.
- Large areas of metal plates without any contact area can act like capacitor plates. For example, a metal plate below the motherboard in a tower PC and the side metal cover can act like capacitor plates. The motherboard is grounded only to the closer plate. The chassis design should minimize the impedance between these two pieces by good electrical contact between the two plates at several locations.

Apertures in a Chassis

Apertures (vents, holes, seams, screens) in a chassis can cause EMI leakage.

- Apertures radiate at wavelengths equal to or less than their length. The length of an aperture is inversely proportional to the leaking resonant frequency.
- Small holes and short seams prevent leakage of low frequencies.
- Circles have minimal width for a given area, so round vents are better than slots (which are typically rectangular).
- Screens are the best vents because of their small hole size.
- Apertures should be shorter than one tenth of the wavelength to be shielded. For instance:
  - A 300-MHz frequency has a 1-meter wavelength, so boxes with harmonics less than 300 MHz can have 10-centimeter apertures.
- A 5.25-inch drive bay is about a 800-MHz to 900-MHz slot antenna and a 3.5-inch drive bay is about a 1-GHz to 1.2-GHz slot antenna.

Shielding

The relative shielding effectiveness of a chassis can be measured by testing the same motherboard along with its associated components in each chassis being considered. In EMI testing it is important to change only one variable at a time.

For most high-frequency fields, a thin shield is sufficient. Lower frequency magnetic fields, however, need thicker ferrous material as a shield.

The permeability of the chassis material and its thickness affect its ability to be an effective shield. For example, Table 2 shows why a copper-nickel paint is used inside of notebook computers for shielding. Copper has high conductivity, to block electric fields and nickel has high permeability, to absorb magnetic fields.

Table 2. Conductivity and Permeability

Material	Conductivity[1] σ_r	Permeability[2] μ_r
Copper	1	1
Aluminum	0.64	1
Steel	0.17	1000
Nickel	0.2	100
Zinc	0.3	1
Chromium	0.65	1
Tin	0.15	1
Stainless	0.02	200

Notes:

1. σ_r = *conductivity relative to copper (Cu = 1).* $\sigma_{Cu} = 5.8 \times 10^7$ *siemens/m*
2. μ_r = *permeability relative to copper (Cu = 1).* $\mu_{Cu} = 1 \times 10^{-7}$ *henries/m*
3. *R= resistance.* $R = 1/\sigma t$ (Ω/m^2), *where t is thickness and* σ *is actual, not relative, conductivity.*

Reflection

Reflection is the key mechanism for controlling high frequencies. The shield provides an impedance mismatch between the incident wave and the barrier impedance. Reflection is the dominant effect for far-field measurements.

Absorption

Absorption is the key mechanism for controlling low-frequency or low-impedance emissions. Absorption requires use of a permeable material. (See Table 2.) Absorption is the dominant effect for near-field measurements.

Calculating Shielding Effectiveness

To calculate shielding effectiveness, use the following equations:

$$A_{dB} = \frac{8.7\frac{t}{\delta}}{\sqrt{\varepsilon_R + 1.41}}$$

$$A_{dB} = 132t\sqrt{f_{MHz}\sigma_r\mu_r}$$

A_{dB} = Absorption loss (dB)

t = Thickness of shield (mm)

δ = Skin depth (mm)

ε_R = Dielectric constant

f_{MHz} = Frequency (MHz)

σ_r = Conductivity (relative to copper)

μ_r = Permeability (relative to copper)

Components, Cables, and Connectors

Much of the noise generated within a PC finds its way out through cables (printer, mouse, monitor, network, serial ports etc.). Therefore, it is important that each of these potential sources have appropriate shielding or filtering.

External cables (RS232 serial, parallel printer, mouse, keyboard, USB, 1394, Ethernet, front-panel LEDs, front-panel controls, etc.) are a prime source of radiated emissions. This is especially true at frequencies less than 150 MHz.

Internal cables can also present EMI problems. In particular, floppy and hard drive cables which connect to the drive bays can conduct noise from elsewhere in the system to the bays, which are generally poorly shielded.

There are three ways to deal with cable EMI—shielding, clamping, and filtering. Shielded cables rely on the Faraday principle and require a good earth ground. Proper connection of the shield is imperative. (See Figure 9 on page 21.) Clamping is simple and cheap. Use ferrite rings or clamps to suppress

magnetic fields. This is a common approach on monitor cables. Filtering the signal before it enters the cable reduces harmonics. Serial ports, printer ports, and network ports often use this approach.

There are several common filtering techniques—power line filters, RC filters, LC filters (using ferrite beads), and connectors with filters built in. Network cards often have complex filters designed for the specific application. The effectiveness of these filters can vary widely from one manufacturer to another. It is important to qualify each part number from its manufacturer.

As a general rule, limit the bandwidth to five times the data frequency. For example, on a serial port with a frequency of 128 Kbits/sec, set the filter roll-off point at around 640 kHz. Often the roll-off point is chosen to be higher to minimize filter component size.

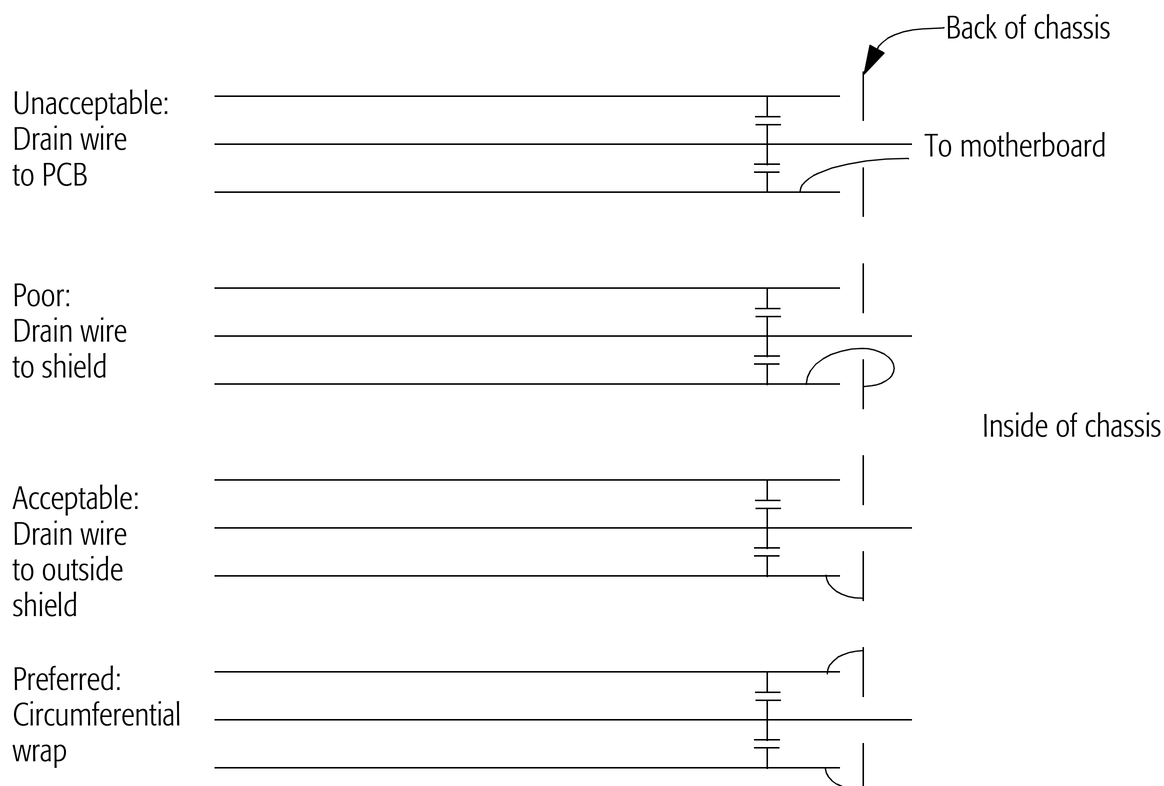


Figure 9. Properly Terminating Cables

High-speed integrated circuits that incorporate drivers capable of directly driving cables (without the need for additional external buffering) may propagate high-frequency components of the clock that is supplied to this integrated circuit. Therefore, the signals that drive the cable should be filtered to minimize this potential source of radiation. If the I/O designer provides separate power pins to the I/O ring, the board designer can provide separate decoupling on these pins. Alternatively the I/O power supply can be isolated from the main system supply.

Peripherals

Network cards, video cards, hard disk drives, CDROMs and other peripheral devices can all be sources of EMI. Although these devices are not addressed in this application note, they cannot be ignored while seeking to minimize EMI.

Power Requirements

Today's microprocessor systems use several different voltages. Proper decoupling (bypassing) is an essential feature of a board designed for good EMI characteristics.

Good decoupling involves attending to several requirements, such as having a good ground system and minimizing ground loops and return current paths. These topics are addressed below.

Ground Plane

The ground plane is often thought of as an ideal reference, but in reality it is far from ideal, having both inductance and resistance. Numerous holes in the ground plane for vias and connectors make matters worse.

One way to minimize EMI is buried capacitance (see Figure 10 on page 24). This technique places the V_{CC} and GND planes very close together (1–2 mils), forming a very good high-frequency capacitor and reducing the number of discrete capacitors required.

Another aspect of this technique is that two V_{CC}-to-GND sandwiches can be used. Benefits of this method include:

- The inductance and impedance of the planes are reduced because there are effectively two planes in parallel.
- Signals on both sides of the board are referenced to a GND.
- The extra voltage plane need not be used for V_{CC}, but could be a V_{DD} plane.
- Because the signals are always referenced to ground, signals never cross a split in the power plane.

Buried capacitance costs more than conventional techniques. However, the cost is partially offset by the reduced number of high-frequency bypass capacitors needed. Bulk decoupling is still required.

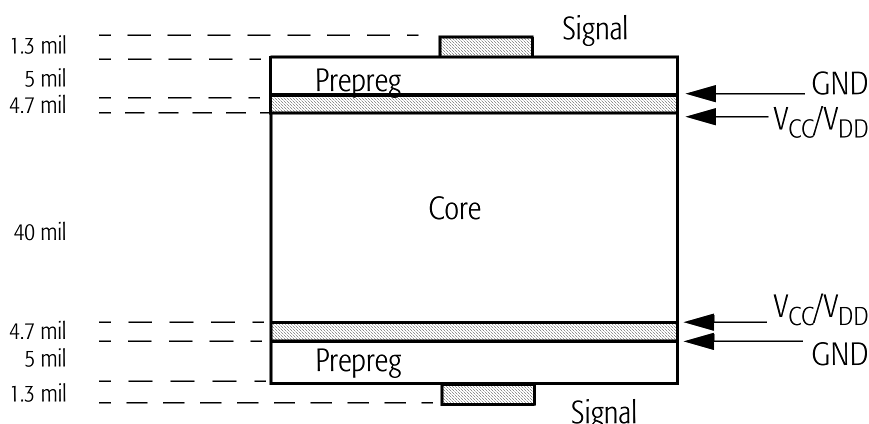


Figure 10. Buried Capacitance

Other Ground-Related Rules

Motherboard Grounding. Connect the motherboard ground plane to chassis ground in one, and only one, location. There are often two available screw holes approximately 2 inches apart near the rear of the chassis that can provide this ground connection. Relative to the size of the board, either connection may be considered a single-point ground connection. Additional ground connections can be achieved by connecting the motherboard ground plane to chassis ground with 0.01 µF capacitors mounted as close as possible to the board I/O connectors (such as the IDE, floppy, serial, and parallel connectors). While this latter method may not always be practical on desktop machines, this can be a useful technique for notebook computers.

External I/O connector shields should be connected to a low-impedance chassis ground on the board. This is extremely important for network connections.

Package Grounding. Each ground pin on a package should be connected to ground by means of its own via. Avoid tying two ground pins on a package together and then to ground.

Adapter Cards. To prevent ground loops in cable shields, an adapter card bracket must not have a DC connection to its ground plane. If the adapter provides an I/O port that connects to an external shielded cable, the adapter ground plane should be connected to the chassis ground of the bracket by means of a 0.01 µF capacitor.

Some adapters contain components—such as audio, network, and video adapters—that require more noise immunity than normal, in which case an isolated ground plane should be used for these particular components. This isolated ground should be connected to the adapter ground plane with a "bridge" that crosses the "moat" that isolates the two planes. This bridge is typically routed in a direction as far away as possible from the "noisiest" component(s) on the adapter. To avoid creating ground loops, signals must be routed over the bridge so that the return currents flow under the signal trace (that is, through the bridge). If there are too many signals for this to be practical, return paths can be created by connecting 0.01µF capacitors between the two ground planes. One capacitor should be used for every eight signal traces, and the signal traces must be as near as possible to the capacitor.

Decoupling and Layout Recommendations

"Coffee Cup" Rule

The coffee cup rule refers to the amount of bulk decoupling distributed around the board. In general there should be approximately 22 µF for every 6–8 square inches of board area. (A coffee cup is about 3 inches in diameter or about 7 square inches.) It is desirable to minimize the distance that charge must travel, so several small capacitors are preferable to a few large ones. For example, one 22-µF capacitor every 7 square inches is preferable to one 100-µF capacitor every 40 square inches.

Adequate bulk decoupling at the power supply connection to the motherboard is also important. Generally from 1000 µF to 3000 µF is required. These capacitors effectively reduce loop area by supplying charge locally on the board rather than from the more inductive path through the power supply wires.

Requirements of specific devices take precedence over these general rules. Follow the manufacturer's recommendations for a specific device.

General High-Frequency Decoupling

Because multi-layer ceramic (MLC) capacitors become inductive as frequencies increase (as illustrated by Figure 15 on page 31) it is important to use both 0.01-µF and 0.001-µF capacitors as part of a high-frequency solution. The number of capacitors to use is a function of the type, speed, purpose, and quantity of the components on the board. An example

calculation is shown in “Calculating Required Number of Capacitors” on page 31.

Each component that sources or receives a clock signal greater than 30 MHz should be decoupled with an additional 300 pF capacitor placed as close as possible to the power pin of that component. Larger capacitors, such as 1000 pF, can be used for additional decoupling for components that run at frequencies less than 30 MHz.

One or more low-ESR 22 µF bulk decoupling capacitors should be used at floppy or fixed disk drive connectors where large DC currents are drawn. Additionally, all +12 V and -12 V loads should be decoupled with MLC capacitors (0.01 µF).

Any connector pin on the board that supplies power (V_{CC} or V_{DD}) should be decoupled with a 0.01 µF MLC capacitor in addition to any bulk decoupling that may be required.

Controlling Switching-Regulator-Induced EMI

The following methods can be used to reduce switching-regulator-induced EMI:

- Add a ferrite bead in series with diodes.
- Add a capacitor across rectifier diodes.
- Use soft-recovery, high-speed diodes.
- Keep leads short and twist the hot and return wire.
- Trade off efficiency for noise by slowing down transistor turn-on time. Noise is reduced but some efficiency is lost. Slowing down is done by using an RC circuit to slow down the base drive of the power transistor.

Power Distribution

In order to maintain a stable voltage supply during fast transients, power planes with high-frequency and bulk decoupling capacitors are required. Figure 11 on page 27 shows a power distribution model for the power supply and the processor. The bulk capacitors (C_B) are used to minimize ringing, and the processor decoupling capacitors (C_F) are spread evenly across the circuit to maintain stable power distribution.

The high-frequency decoupling capacitors (C_F), which are typically smaller in capacitance and equivalent series inductance (ESL) than the bulk capacitors (C_B), maintain the voltage output during average load change until C_B can react.

See "High-Frequency Decoupling Calculations" on page 30 for more information.

See the power supply design application note (*AMD-K6® Processor Power Supply Design*, order# 21103) for desktop processor-specific decoupling requirements. See *Mobile AMD-K6® Processor Power Supply Design*, order# 21677 for mobile processor-specific decoupling requirements.

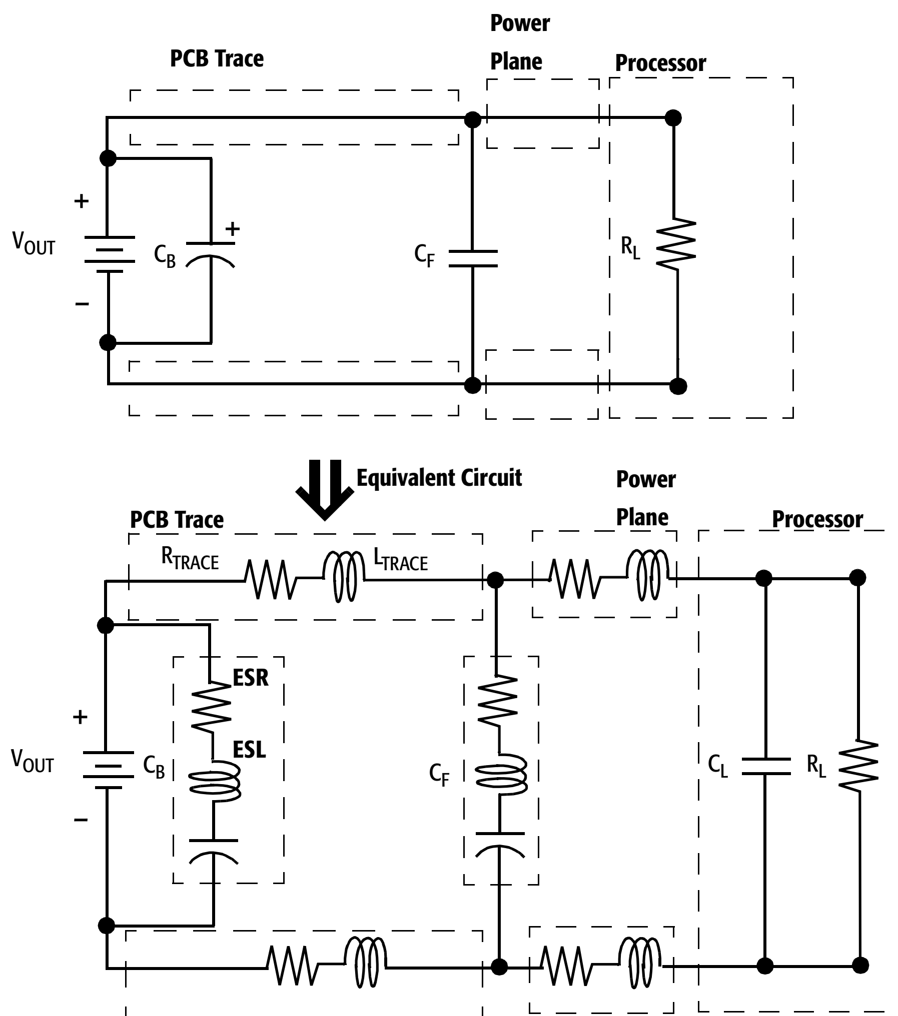


Figure 11. Power Distribution Model

Decoupling Capacitance and Placement

The high-frequency decoupling capacitors (C5 to C31), in Figure 12, should be located as close to the processor power and ground pins as possible. To minimize resistance and inductance in the lead length, it is recommended to use surface mounted capacitors. When possible, use traces to connect capacitors directly to the processor's power and ground pins. In most cases, the decoupling capacitors can be placed in the Socket 7 cavity on the same side of the processor (component side) or the opposite side (bottom side).

Figure 12 shows a suggested component placement for the decoupling capacitors. The split voltage planes should be isolated if they are in the same layer of the circuit board. To separate the two power planes, an isolation region at least 0.254 mm (0.01 in.) wide is recommended. Do not split the ground plane.

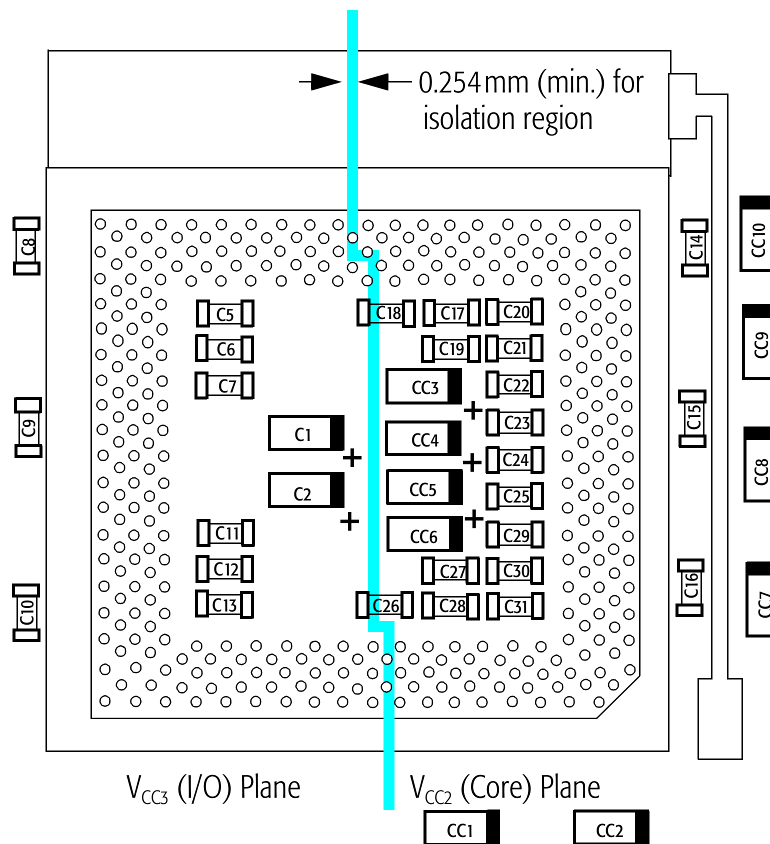


Figure 12. Suggested Component Placement

Capacitors from different manufacturers may vary greatly in resistance. Table 3 compares parts of equal capacitance but different manufacturers. It is important to check manufacturer's specifications.

Table 3. Representative ESR Values

Capacitance	Manufacturer 1	Manufacturer 2
470 µF	55 mΩ	100 mΩ
270 µF	70 mΩ	100 mΩ
100 µF	90 mΩ	100 mΩ
68 µF	95 mΩ	100 mΩ
47 µF	120 mΩ	250 mΩ

Via Inductance

Vias act as inductors. Via inductance can be reduced when using double-sided component assembly. Components can share vias on the top and bottom sides, reducing the effective via inductance. Double-sided assembly is rarely used in desktop systems, so this technique is more commonly used for portable systems.

Parallel vias can also be used to reduce via inductance (see Figure 13). This technique is usually used on bulk decoupling capacitors. The inductance contribution numbers shown in Table 4 indicate that a poor layout can negate the effect of a good component.

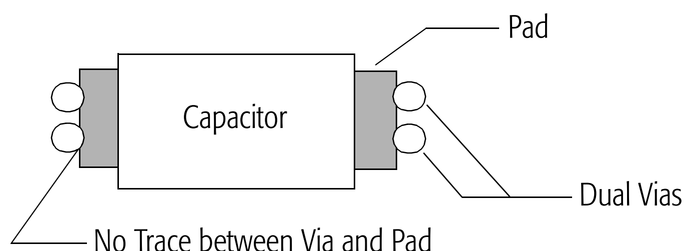


Figure 13. Via Layout for Low Inductance

Table 4. Inductance Contributions of Components

Component	Induction	Comment
Capacitor	0.6 nH (approximately)	ESL
Via	0.7 nH (approximately)	–
100 mil long trace	1.6 nH (approximately)	10 mil wide trace

Aluminum electrolytics can be used instead of tantalum capacitors, as long as good-quality, low-ESR parts are used. The biggest problem with aluminum electrolytics is the large decrease in capacitance as they age. Aluminum electrolytics rated for –40 to +105 degrees C generally have better aging characteristics when operated in the 0 to +70 degrees C range.

High-Frequency Decoupling Calculations

Inductance is also a concern for the high-frequency decoupling capacitors. Case size can be a significant factor affecting capacitor inductance. For example, a 0603 case has significantly more inductance than a 0612 case. AMD recommends the 0612, 1206, 0805, and 0603 cases in order of preference (best to worst).

Inductance can also be reduced by directly connecting the capacitor to the power pin of the processor. In order to minimize inductance, the trace must be short and as wide as possible. This technique effectively removes two via inductances between the capacitor and the processor as shown in Figure 14. The dotted line shows that connecting the capacitor directly to the processor eliminates two series inductances. However, this trace also has inductance—if it is too long or too narrow it can be worse than the vias.

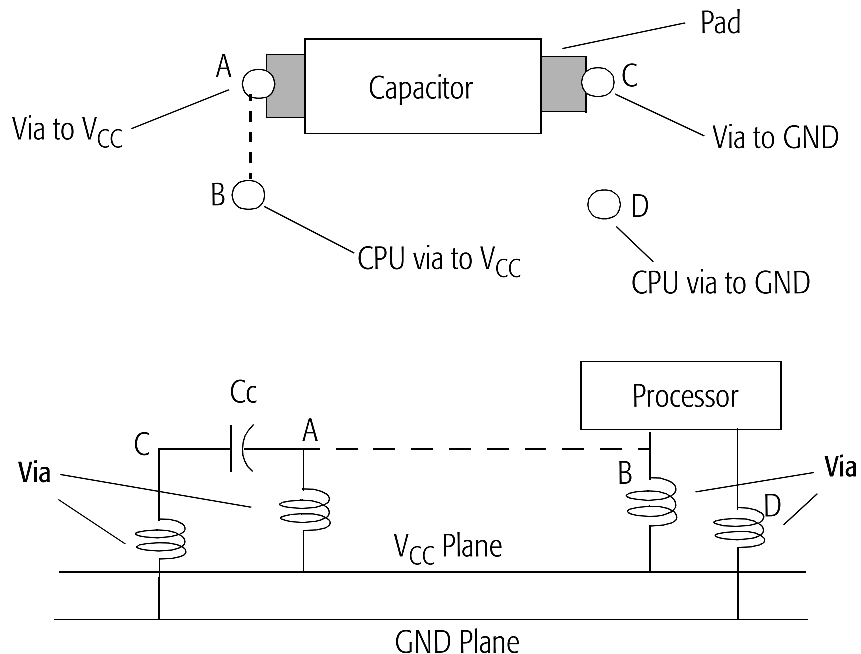


Figure 14. Decoupling Inductance

Figure 15 shows the effect of inductance on a capacitor at higher frequencies. (The numbers outside the X and Y axis indicate the minimum and maximum values plotted). The inductance used is 1.8nH (two times 0.7 nH for the vias and 0.4 nH for the capacitor itself). The first capacitor (c1) is a 0.1-µF X7R multilayer ceramic (MLC). The inductance of a capacitor is a function of the case type. An 0612 case is assumed here. (For a 1206 case use 0.8 nH for the inductance.)

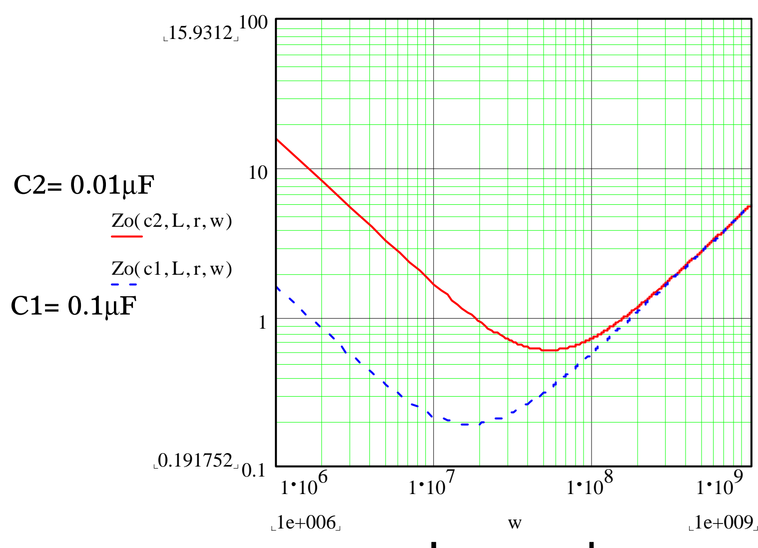


Figure 15. X7R Capacitor Impedance versus Frequency

Calculating Required Number of Capacitors

The following examples show how to calculate the required number of capacitors. Examples 1 and 3 describe calculations ignoring capacitor inductance, while examples 2 and 4 consider capacitor inductance. Often capacitor inductance is ignored the design process, but these examples show that the number of capacitors required is strongly influenced by their inductance.

Example 1. To determine the required number of capacitors for a core design, ignoring capacitor inductance:

1. Determine the ripple voltage budget. In this example, the ripple-voltage budget (dv) is 30 mV.
2. Measure the AC transient current, both amperage and duration. This transient current has an amperage (I, di) of 0.75A, and typical duration (dt) of 2.5 nsec.

3. Calculate the total capacitance required:

   $I = C\,(dv/dt)$

   $C = I\,(dt/dv) = 0.75A\,(2.5nsec/30mV) = 0.0625\ \mu F$

4. Choose the size of capacitor to be used (S). In this case, 0.01-µF.

5. Calculate the required number of capacitors (N), ignoring capacitor inductance.

   $N = C/S = 0.0625\ \mu F/0.01\ \mu F = 6.25$

   Six 0.01-µF capacitors would be needed, if capacitor inductance were ignored.

Example 1A. To determine the required number of capacitors for a core design, considering the capacitor's inductance:

1. As above.

2. As above.

3. Calculate the induction budget (L).

   $V = L\,(di/dt)$

   $L = V \bullet dt/di = 30\ mV \bullet (2.5\ nsec/0.75\ A) = 100\ pH$

   The allowed budget is 100 pH per capacitor.

4. Calculate the via inductance per capacitor. Each capacitor usually has two vias (one on each end, with an inductance of 0.7 nH each), and inductance inherent in itself (0.4 nH), the effective via and capacitor inductance must be:

   $2 \bullet 0.7nH + 0.4nH = 1.8nH$

5. Calculate the number of capacitors required (N):

   $N = 1.8nH/100pH = 18$

   The number of capacitors required is 18 considering capacitor inductance (not six, as calculated while ignoring it).

Example 2. To determine the required number of capacitors for I/O decoupling, without considering inductance:

1. Determine the ripple voltage budget. In this example, the ripple-voltage budget (dv) is 145 mV because the I/O drivers are not as sensitive to supply variations as the core, and the current transient is smaller.
2. Take a typical value for I_{CC3}, both amperage and duration, for instance an amperage (I, di) of 0.5A, and typical duration (dt) of 2.5 nsec.
3. Calculate the total capacitance required:

   $I = C\ (dv/dt)$

   $C = I\ (dt/dv) = 0.5\ (2.5nsec/145mV) = 0.0086\mu F$

4. Choose the size of capacitor to be used (S). In this case, 0.1-µF.
5. Calculate the required number of capacitors (N), ignoring capacitor inductance.

   $N = C/S = 0.0086\ \mu F/0.1\ \mu F = 0.086$

   One 0.1-µF capacitor is needed, if capacitors did not have inductance.

Example 2A. To determine the required number of capacitors for I/O decoupling, considering inductance:

1. As above in example 3.
2. As above in example 3.
3. Calculate the induction budget (L).

   $V = L\ (di/dt)$

   $L = V \bullet dt/di = 145\ mV \bullet (2.5\ nsec/0.5\ A) = 725\ pH$

   The allowed budget is 725pH.

4. Calculate the via inductance per capacitor (C). Each capacitor usually has two vias (one on each end, with an inductance of 0.7 nH each), and inductance inherent in itself (0.4 nH), so the effective via and capacitor inductance is:

   $2 \bullet 0.7nH + 0.4nH = 1.8nH$

5. Calculate the number of capacitors required (N):

   `N = C/L = 1.8 nH/725 pH = 2.5`

   Three capacitors are needed on the I/O, considering capacitor inductance. AMD recommends using a minimum of six capacitors, because voltage pins (V_{CC3}) are distributed in groups around the package and it is preferred to have a capacitor near each group.

Decoupling: Rules of Thumb

- A 0.1 µF capacitor maintains its capacitive properties up to approximately 20 MHz.
- A 0.01 µF capacitor maintains its capacitive properties up to approximately 100 MHz.
- **Caution**: *Do not put unequal capacitors next to each other because they can cross resonate and cancel each other out at a frequency between their respective self-resonating frequencies and leave a hole in the EMI filtering.*
- Use one 22 µF bulk decoupling capacitor per 7 square inches of board (the coffee cup rule).
- Use bulk and high-frequency capacitors at power input (i.e., where the cable attaches to the motherboard). This reduces high frequencies and transient currents in the cable.
- Use bulk and high-frequency capacitors at headers and connectors that carry power.
- By positioning the vias (A and B) as shown in Figure 16, EMI is reduced. The traces to these vias should be as short and wide as possible. Another good topology is to put one via under the component and the second via adjacent to it (as in the right side of Figure 16). It is usually not advisable to put both vias under the capacitor because this can cause short circuits during manufacturing.

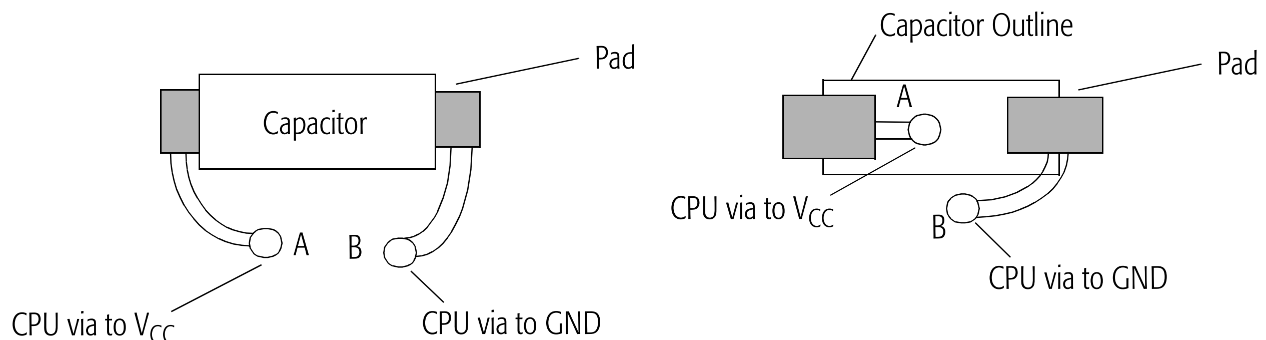


Figure 16. Good EMI Structure

PC Board Layout Guidelines

These guidelines are general high-speed rules. They are not meant to supplant the use of good signal integrity tools.

Component Placement

The motherboard designer must take great care in placing the components because the placement affects so many aspects of the entire system design, including EMC, routing, thermal considerations, manufacturability, and cost. Following are some general placement and board design considerations that minimize EMI.

All components, buffers, and filters associated with external I/O connectors should be placed as close as possible to their corresponding external connectors. The motherboard specification usually requires that all such connectors are placed along the same edge of the board.

Components that source and/or receive clock signals should be placed to minimize clock trace lengths, and to avoid the routing of all clock signals (and their derivatives) near components that can propagate EMI radiation, such as internal and external connectors. Routing clock traces in the center of the board avoids running these traces near the external connectors which are placed near the edge of the board. In addition, clock signal termination may be required as described in “Chipset and Clock Chip EMI” on page 13.

Isolated ground planes can employed as described in “Other Ground-Related Rules” on page 24 to improve noise immunity to those components that require such isolation.

From an EMC perspective, all power should be distributed via a plane. This is not always cost effective when multiple power supplies are used. For support voltages such as +12 V, -12 V, and -5 V the power traces should be made as wide as possible to reduce wiring inductance to a minimum.

Layout/Routing Rules

- Use 45-degree angles or smooth curves, in order to minimize signal reflection. Sharp corners have a high field strength. (See Figure 17.)

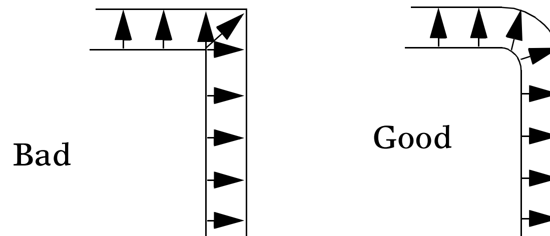


Figure 17. Electric Field Concentrations

- Avoid stubs, tees, vias, or sharp 90-degree turns, all of which cause impedance discontinuities.
- Minimize the number of signals that cross power domains. Each power plane should have high-frequency decoupling capacitors between the planes to provide a return path for signals that cross from one domain to another.
- Consider using buried capacitance power/ground planes. This technology reduces high-frequency bypass capacitor count. Unfortunately, this technology is expensive and of limited availability. The added cost can be partially offset by savings in high-frequency capacitors.
- Use all available power and ground pins. This may seem obvious but it is not always done. Some schematic symbols define V_{CC} and GND connections implicitly so they are not visible on the schematic. Therefore, it may not be apparent that some are missing. It is preferred to specify power and ground explicitly on the schematic.
- Consider board stackup order. It is preferable to have the ground plane as close as possible to the components. Place the V_{CC} plane towards the bottom side of the board.
- Border the PCB with chassis ground or place the V_{CC} plane back from the edge of the board by three times the distance between planes.
- Microstrip should only be used for short traces, traces with slow rise time signals, and where driver and load are isolated from clocks. (In practice, Microstrip is used for all signals and clocks.)

- Stripline should be used when possible. It is especially desirable for clocks. (In practice it is rarely used on 4-layer boards.)
- Keep clock chips or clock lines away from the edges of the board.
- Minimize the trace length of clock lines.
- Use a daisy-chain wiring approach (point-to-point) for clocks and other critical signals. Avoid wiring clock lines with stubs, and minimize the number of vias.
- Keep clocks and other high-frequency signals at least one-tenth of an inch away from I/O signals and connectors.
- If a clock signal must be routed through a connector, it should be shielded with ground (or power) to reduce the potential for EMI.
- While not always practical on PC motherboards for cost reasons, if the board contains signal layers that are imbedded internally between ground and power planes, all clock signals should be wired on these internal signal layers.
- Avoid running traces under crystals, clock chips, or other “hot” circuits. (Hot in the EMI sense means noisy, high frequency, or high energy, not high temperature.) A good way to ensure this is to put a cross-hatched ground plane on the surface under the oscillator/clock chip, which prevents crosstalk between the clock and signals.
- To minimize crosstalk, use a trace spacing-to-height ratio greater than two. Unfortunately, this is seldom practical due to space constraints. Usually, the designer must settle for approximately 1:1. Good signal integrity tools are important in this context.
- Put line drivers and receivers near the port they drive. Put filters as close to the connector as possible to prevent unwanted signals coupling into the output of the filter.
- Use ferrites or low pass filters on signals that go to an external cable.
- Route differential pairs together, so their lengths are matched and any common-mode noise is cancelled out.
- Vias should be staggered (not in a line). When vias are in a line, the Anti-pad (or clearance) can create slots in the power and ground planes. These slots increase the return current paths, increase the inductance of the plane, and result in higher EMI.

Return Current Paths

Figure 18 shows the return currents for a trace that changes layers and crosses a gap in a plane. Either situation creates an impedance discontinuity. Every impedance discontinuity represents a potential source of EMI because of the displacement currents generated in the return path.

Minimize the number of transitions between layers. If possible, traces should not change layers, especially not clock lines.

If a signal crosses a split V_{CC} plane, high-frequency capacitors should be added between the two planes to provide a return path. Remember that the V_{CC} plane acts as the AC return path for the signals routed over it. The AC return path is directly under the signal trace. It is not the most direct (shortest) path as shown in Figure 19 on page 39.

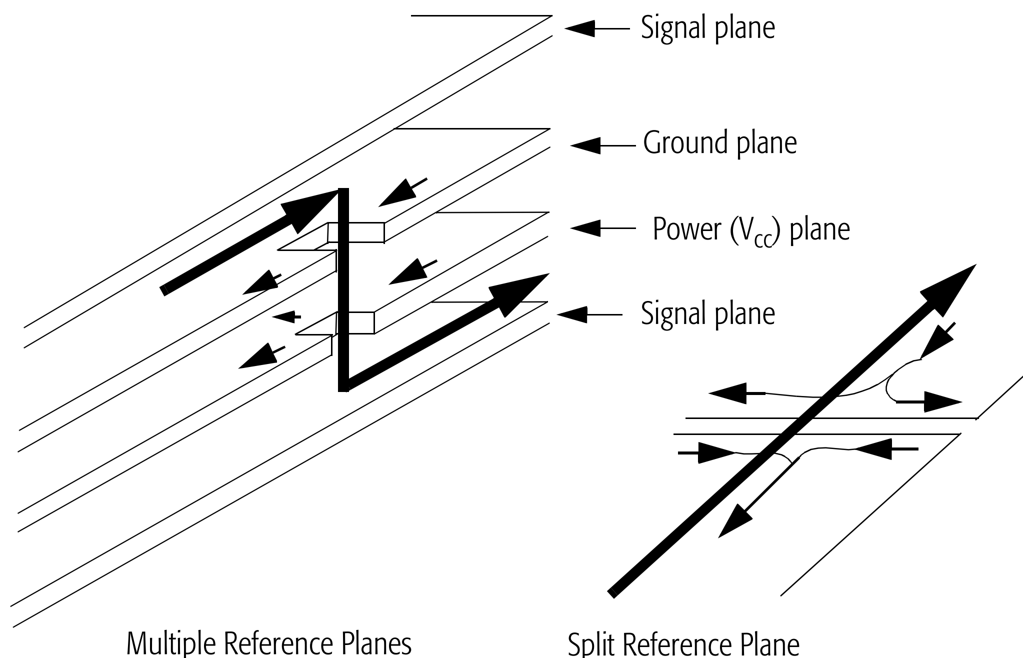


Figure 18. Return Currents

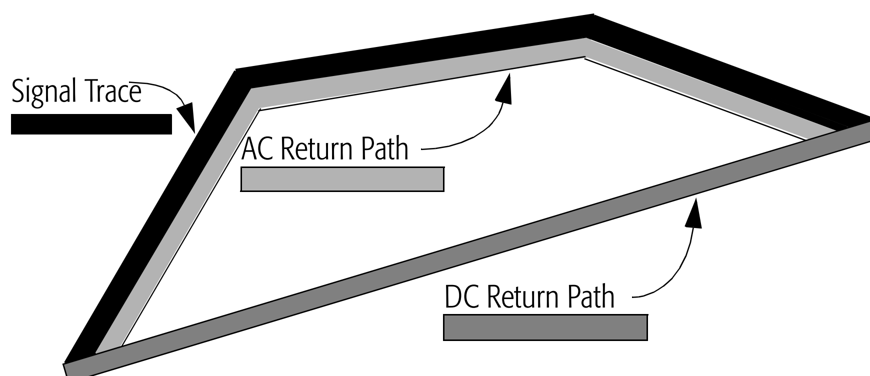


Figure 19. AC Return Path versus DC Return Path

Figure 19 represents a view looking down at the top of a PC board. The black line is the trace. The light gray line represents the AC return current path on the ground or V_{CC} plane under the trace. The darker gray line is the DC return path.

Ground Plane Permeability

It is important to remember that the ground plane is not ideal. Vias and connectors put holes in the ground plane and raise the impedance of the plane.

Keep ground impedance as low as possible. Avoid excessive clearance around vias and through-hole components, which can create a slot (usually around a connector). Excessive clearance increases the inductance of the plane, increases loop area, and makes a slot antenna. If vias are necessary, stagger them to avoid creating slots.

There are two grounding philosophies: single-point and multi-point. Single-point grounding is preferred for low frequencies where ground loops are a problem. However, it is not practical for high frequencies where parasitic capacitances and inductances provide unwanted coupling paths. The screws connecting the motherboard to the case near the back connectors are an example of single-point grounding, the rest of the board being supported by plastic standoffs.

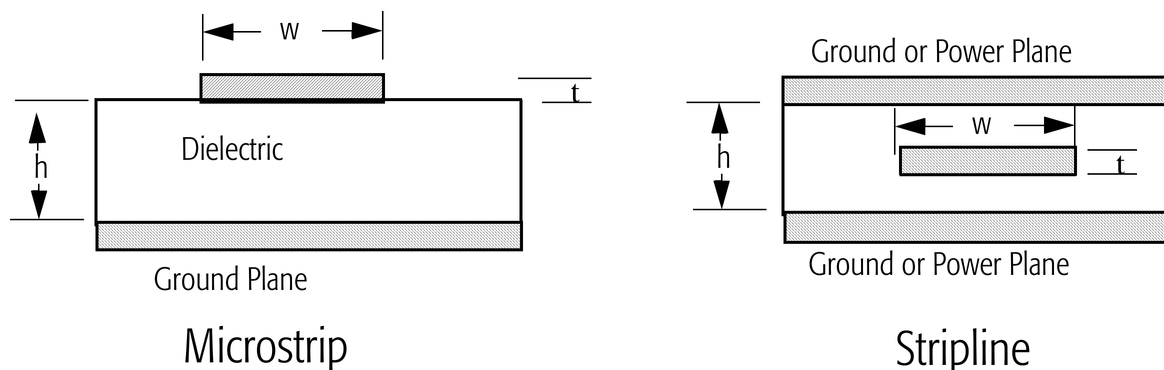
Multi-point grounding is preferred at high frequencies as it tends to reduce common mode noise. Having screws near the oscillator connecting the board to the case, as well as the motherboard screws mentioned above, would be an example of multi-point grounding.

Power and ground serve as signal reference planes in which return currents flow. However, these returns are both electromagnetically and electrostatically discontinuous. Therefore, effects other than reflections and jitter distortion can be expected to take place as the return current changes from conduction to displacement current.

The arrows in Figure 18 on page 38 indicate the directions of energy and current flow.

Cost constraints usually preclude the use of six-layer boards, but an example is included here because six-layer designs allow the designer to bury the high-speed clocks between the planes. This effectively encloses the clock lines in a Faraday cage.

Stripline traces have a lower impedance and slower propagation delay than Microstrip. Stripline controls radiated noise by containing all of the clock nets in a dedicated layer between two radio frequency (RF) ground planes, which also reduces crosstalk and other radiated noise effects.



Clocks in Microstrip - faster, more precise
Dedicated clock layer - less radiated noise

Figure 20. Microstrip versus Stripline

Microstrip

Microstrip technology puts the signal trace on top of the ground. Its propagation delay is approximately 56.3 psec/cm = 143 psec/in = 1.7 nsec/ft. Its impedance is approximately 40 to 90 ohms.

Microstrip impedance is calculated as follows:

$$Z_0 = \frac{87}{\sqrt{\varepsilon_R + 1.41}} \ln\left(\frac{5.98h}{0.8w + t}\right)\Omega$$

Where:

Z_0 =Characteristic impedance

ε_R = Dielectric constant

h = height of line above base

t = thickness of trace

Microstrip propagation delay is calculated as follows:

$$T_{pd} = 33.36(0.475\varepsilon_R + 0.67)^{(1/2)}\frac{ps}{cm}$$

$$T_{pd} = (1.017)(0.475\varepsilon_R + 0.67)^{(1/2)}\frac{ns}{ft}$$

Where:

T_{pd} = Propagation delay

ε_R = Dielectric constant

Stripline

Stripline technology puts the signal trace in the ground. Its propagation delay is approximately 70.8 psec/cm = 180 psec/in = 2.16 nsec/ft. Its impedance is approximately 20 to 55 ohms.

Stripline impedance is calculated as follows:

$$Z_0 = \frac{60}{\sqrt{\varepsilon_R}} \ln\left(\frac{4h}{0.67\pi\left(0.8 + \frac{1}{w}\right)}\right)\Omega$$

Where:

Z_0 = Characteristic impedance

ε_R = Dielectric constant

h = thickness of dielectric

w = width of trace

Stripline propagation delay is calculated as follows:

$$T_{pd} = 33.36(\varepsilon_R)^{(1/2)}\frac{ps}{cm}$$

$$T_{pd} = (1.017)(\varepsilon_R)^{(1/2)}\frac{ns}{ft}$$

Where:

T_{pd} = Propagation delay

ε_R = Dielectric constant

Trace Length Calculation

Terminate a trace if its electrical length is greater than half of its rise time. Electrical length is calculated as follows:

$$Length = \frac{T_r}{2\sqrt{LC}}$$

Where:

T_r = Signal rise time

L = Inductance per unit length (approximately 6.4 nH/in)

C = Capacitance (approximately 2.6 pF/in for a 50 ohm line)

For a T_r = 1 nsec this works out to 3.87 inches as the maximum unterminated length.

The Figure 21 stackups are dimensioned to yield a 50 ohm trace impedance. Notice that a 6 layer board gives the designer the ability to have better shielding on the inner traces. Therefore, the highest frequencies should be put on them.

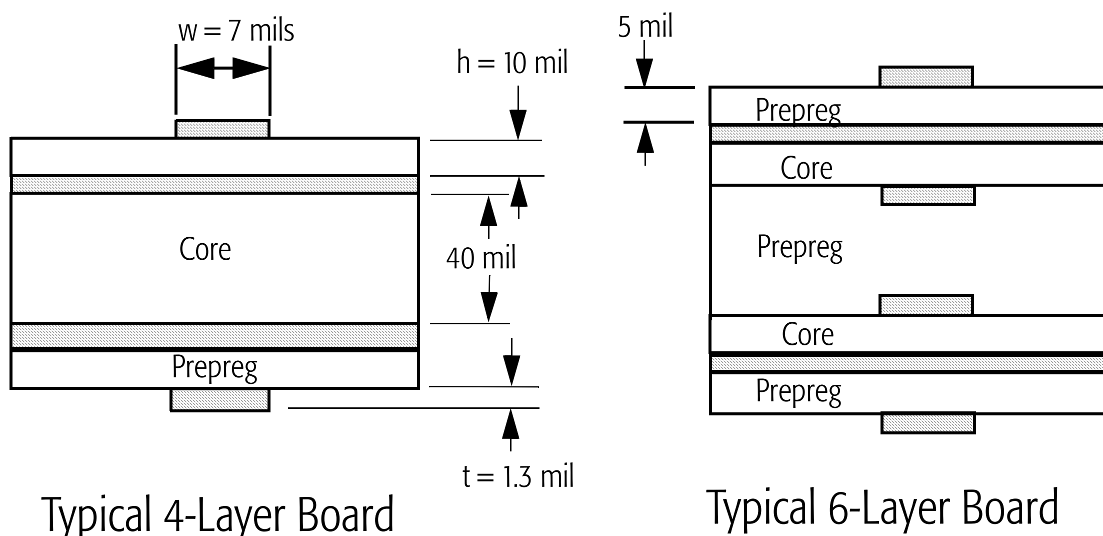


Figure 21. Board Stackup for 4-Layer and 6-Layer Boards

Figure 22 on page 45 illustrates the benefit of having a power or ground plane in close proximity to the signal. With no reference plane the fields spread, causing more crosstalk and radiation. Adding a plane contains the fields, reducing radiation and crosstalk. Using two planes provides even more containment.

Note: *Plots are to scale.*

To minimize fringing effects at the edge of the board, it is important to keep the signal line away from the edge of the board. The recommended distance is 3h (h = height above the ground plane). If h = 10 mils, then no signal should be closer than 30 mils to the edge of the ground plane.

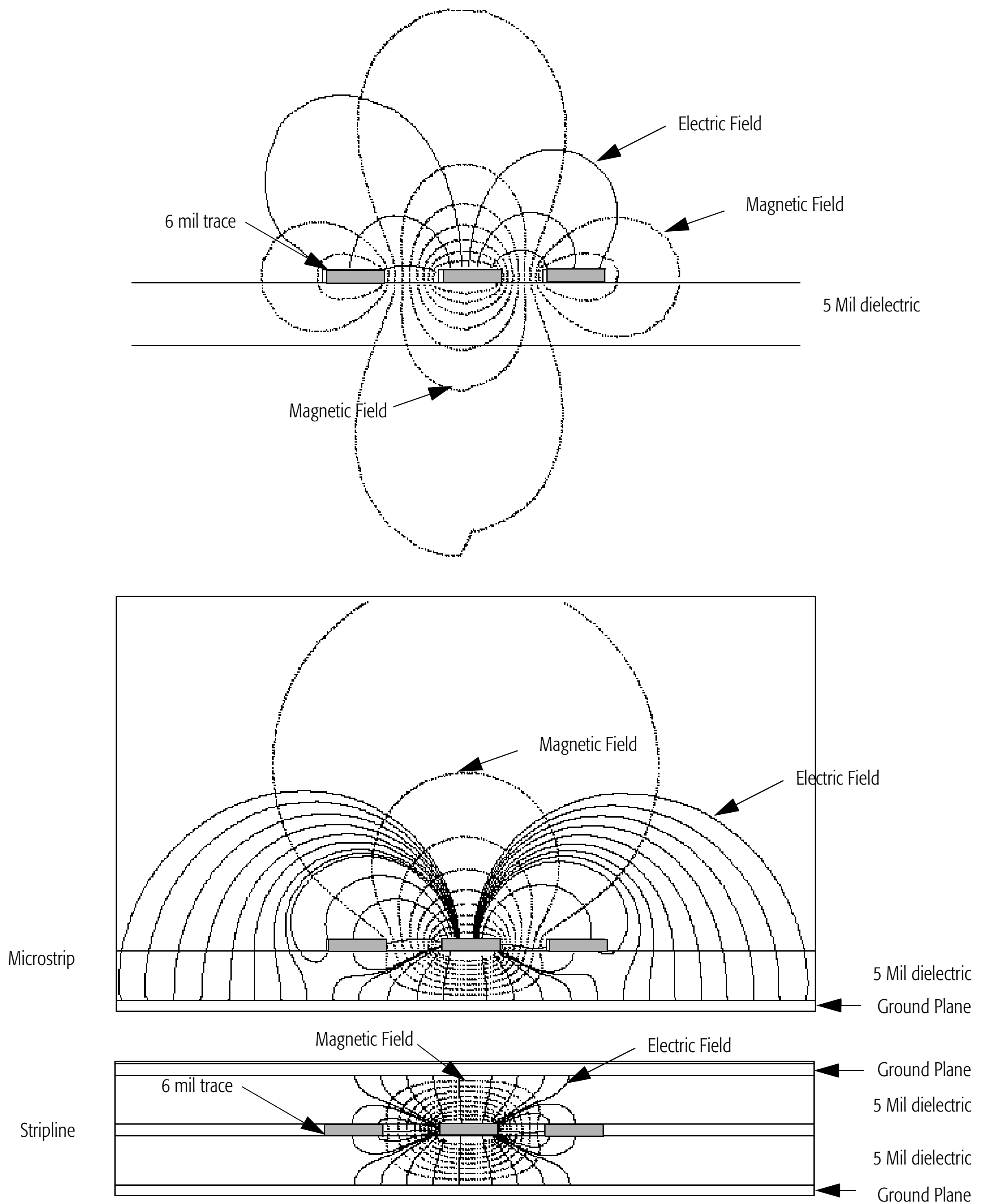


Figure 22. Electric (E) and Magnetic (H) Fields

General Guidelines Summary

The following general guidelines should be applied to system implementation:

- Use the lowest current drivers possible.
- Use the programmable drive current in devices that have this feature.
- Slow the edge rates. Source-terminated series resistors are an effective technique to reduce high-frequency harmonics.
- Minimize the number of high-speed clocks. Turn off clocks to unpopulated memory sockets.
- Reduce the voltage swing if possible. Use the lowest voltage possible. Use SDRAM for its lower voltage swing in addition to its better performance.
- Terminate when possible. This way the signal energy will be absorbed rather than reflected.
- Use good capacitors. Avoid using Z5U dielectric capacitors. AMD recommends using X7R or NPO capacitors, in that order. X7R is the best performance for the cost today. While small values of NPO are more effective filters than X7R, NPOs are not more effective for larger values (above 1000 pF). The SpiCap software available at the AVX website (www.avxcorp.com/software/) is a good tool for evaluating different capacitor types and values.
- Minimize inductance in series with capacitors. First choose a capacitor with low inductance, then use a trace as wide as practical to connect it directly to the device's power pins if possible. AMD recommends using 0612, 0603, 1206, and 0805 packages, in that order (without regard to cost). The 0612 has about half as much inductance as the 0603, allowing capacitors to be more effective at a higher frequency. Because 0612 capacitors are more expensive than 0603 capacitors, they are rarely used. Careful selection (using SpiCap) of an 0603 can give good results. (For some ranges of values, a 0603 has lower inductance than a 0612.) In Figure 15 on page 31, the slope of the right side of the plot is a function of the capacitor inductance and the trace or via that connects it.

- Use low-ESR bulk decoupling capacitors. Often ESR is not specified on the bill of material, so cheaper parts are used and the system fails EMI or functionality tests. Lower ESR aluminum electrolytics can pay for themselves, because fewer are needed and they deteriorate less with age, which reduces field failures.
- Put an EMI filter on the input of the DC–DC core supply. The EMI filter on the input to a DC–DC converter usually consists of a 1-µH inductor and a 0.1-µF capacitor. There is usually some bulk decoupling as well.

Appendix

Termination Strategies

Kinds of Termination

- Series termination: For best EMI characteristics, the series resistor should be 75–100 ohms, not 22–33 ohms (this needs to be balanced against the timing requirements of the signal).
- Diode termination: Diodes must be Schottky to be effective, others are just too slow.
- RC termination: This method terminates the signal transition and therefore should be calculated based on the edge rate. This method's disadvantage is that two components are needed for each line. Termination packs are sometimes used to reduce component count. Be aware that signal coupling can occur between signals in the termination pack.
- Parallel termination: Rarely used due to high static power, but it yields the best signal quality (sometimes called a Thevenin termination).

General Termination Advice

- Misplaced terminators are a common problem.
- The logic or circuit designer must work closely with the layout designer.
- Modern CAD tools help as they allow associating a terminator with a device at the end of the line.
- Table 5 provides some guidelines for termination.

Table 5. Estimates of Maximum Trace Length

Signal rise time (T_r) in nsec.	Maximum unterminated trace length in inches
0.75	2.2
1.5	4.3
3.0	9

Debug Chart

Table 6 can serve as a guide for solving EMI problems. It is helpful to make a chart of your own and add problems and solutions as you find them. This will become a more useful tool as time goes on.

Table 6. Fixing Signal Problems

Problem	Probable Cause	Solution
Excessive overshoot	Impedance mismatch on destination	1. Terminate line at destination. 2. Use slower driver.
Bad DC voltage level	Too much load on the line	1. Replace DC termination with AC termination. 2. Use higher current driver.
Too much crosstalk	Too much coupling between lines	1. Use slower risetime on active driver. 2. Terminate at receiver. 3. Reroute wires. 4. Check ground plane for excessive vias and slots.
Signal too slow	Trace too long	1. Reposition components and reroute.
	Not switching on incident wave	1. Check for series termination. 2. Use impedance-matched driver. 3. Use alternate routing scheme.

Crosstalk

Crosstalk (see Figure 23 on page 50) is the coupling of a signal from one trace onto another trace. It is one of the key mechanisms by which high-frequency noise is coupled onto signals which go out onto cables (mouse, keyboard, etc.). The closer together the culprit and victim lines are, the worse the crosstalk. To minimize crosstalk, add guard traces (on plane), or route traces at right angles on adjacent planes.

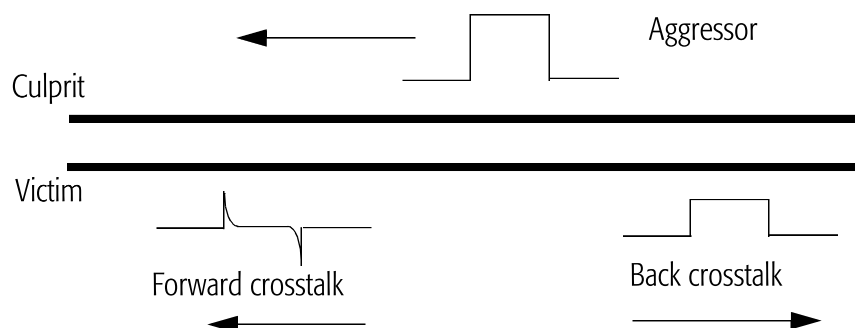


Figure 23. Crosstalk

Forward crosstalk looks like a differentiated aggressor signal, and travels in the same direction. Forward crosstalk is capacitive (caused by capacitance between two layers). It is dominated by the electric field (for example, one trace above another). Although the signal voltage is the coupling mechanism, current is what is transferred to the victim line.

Back crosstalk has the same characteristics as the aggressor signal, but travels in the opposite direction. Back crosstalk is inductive (caused by mutual inductance of adjacent lines). It is dominated by the magnetic field (for example, one trace next to another). Although the signal current is the coupling mechanism, voltage is what is transferred to the victim line.

Simulation

EMI is directly related to signal integrity: the cleaner the signal, the less noise generated. Simulation early in the design phase is critical to minimizing EMI. However, simulation is only as good as the models used. Therefore, it is important to verify (correlate) models.

The following is a list of available simulation tools:

- XNS, Quiet—Viewlogic (Cooper & Chyan Technology)
- Synthesolve—Unicad
- Maxwell SI SpiceLink, Extractor—Ansoft

- LineSim—HyperLynx
- Net View—Integrity Engineering
- GreenField—Quantic
- Polaris—MicroSim
- PCBSI—Pacific Numerix
- DF Noise—Cadence
- BoardStation—Mentor
- Interconnect Synthesis—Interconnectix

Shielding Methodology

- Start with a visual inspection to ensure that:
  - Cable connections are good
  - Seams or openings are closed
  - Internal cables are placed to minimize coupling
  - Cables are shielded or filtered
- Use a near field probe to determine:
  - Where chassis leaks are located
  - Which devices are noise sources
  - Whether the power switch is an emissions source (it often is)
- Eliminate as many variables as possible:
  - Remove cables if possible
  - Shield suspect areas with conductive tape or aluminum foil
- Add fixes one at a time and leave them on while continuing. Often there will be several problems, and the cure is not found until all the problems are fixed.
- When a solution is found, remove fixes one at a time to eliminate unnecessary fixes.

Transmission Line Effects

- Propagation velocity determines delay as follows:

$$V_0 = \frac{300 \bullet 10^6}{\sqrt{\varepsilon_R}}$$

- Impedance determines the shape of incident waves.
- Driver characteristics affect the edge shape.
- Discontinuity in the line causes signal reflections.

Emission Limits

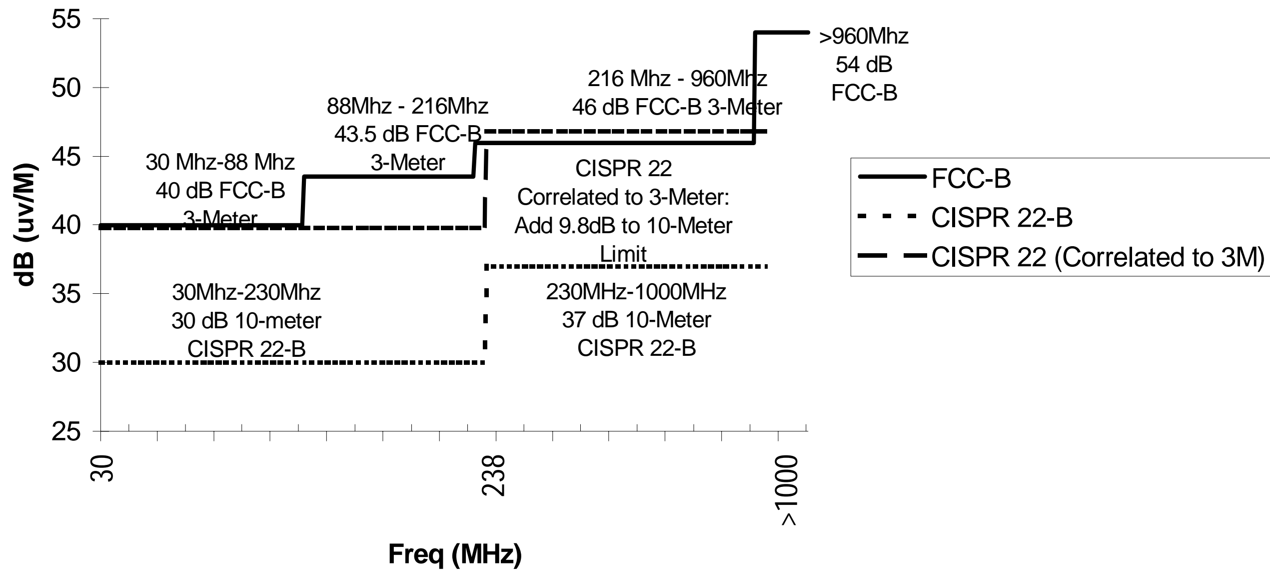


Figure 24. Radiated Emissions Standards: Class B, 3 and 10 Meter

Table 7. Class B Radiated Emissions Standards

Frequency (MHz)	3 Meter Limit (dB)		10 Meter Limit (dB)	
	FCC	CISPR 22	FCC	CISPR 22
30 - 88	40	39.8	30	30
88 - 216	43.5	"	33	"
216 - 230	46	"	35.6	"
230 - 960	"	46.8	"	37
<960	54	"	"	"

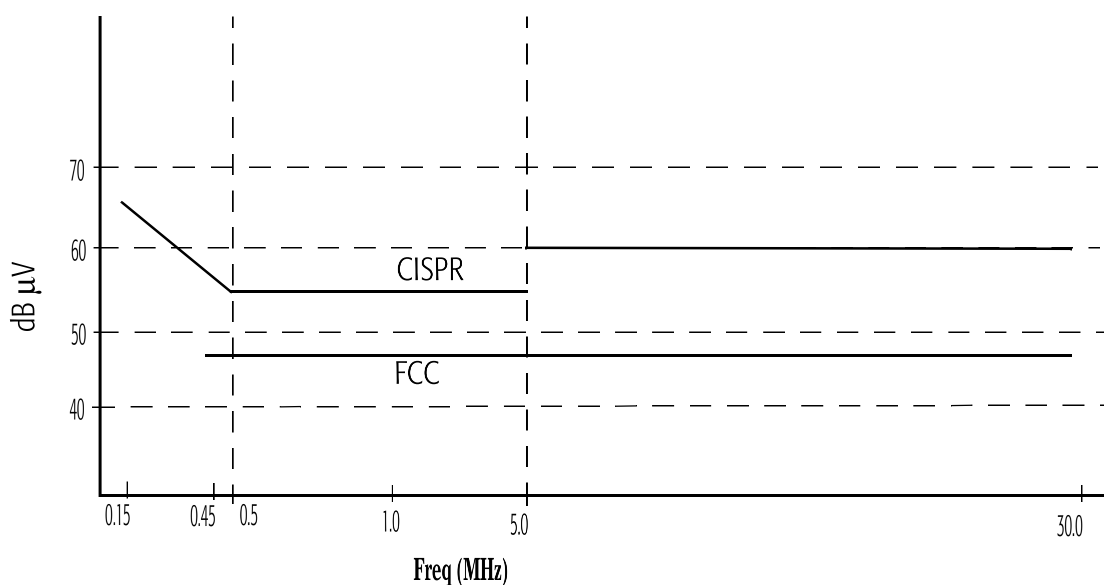


Figure 25. Conducted Emissions Standards: Class B

Table 8. Class B Conducted Emissions Standards

Frequency (MHz)	CISPR 22 (dB)	FCC (dB)
0.15 - 0.45	66 - 56[1]	--[2]
0.45 - 0.50		48
0.5 - 5	56	"
5 - 30	60	"

1. Varies linearly from 0.15 to 0.50 MHz.
2. No FCC standard for this range.

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